1. Overview

This document is intended to describe the following for the SIMADYN D operating system:

- Allocation and Term Definition,
- Briefly Describe its Basic Functions,
- Summarize its Capability Parameters,
- Describe the Operating System Interfaces.

The tasks of this operating system are defined in general as follows:

"The Operating System is the Sum of all those Programs that are Required as Components of a Electronic Data Processing System for the Operation of that System and the Execution of User Programs" /1/.

It permits the utilization of hardware functions for the user programs. This is shown in the layer diagram of diagram 1.

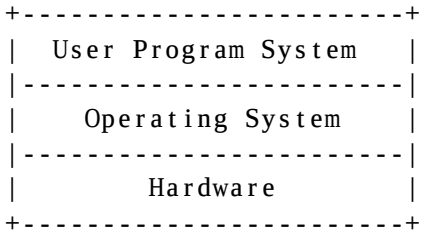

Diagram 1 Layer Architecture

The mode of operation is differentiated by the operating system, as follows:

The Stack Mode,
The Dialog Mode or
The Real Time Response.

The real time operating system is characterized as a system, which is set especially high demands with regard to the reaction time /1/.

This type of operating system permits real time processing. It is the "Mode of Operation of a Processing System", by which the programs must be capable of processing the arriving data and been constantly ready to supply the processing results within a certain period.

The data can occur, dependent upon the application, with a temporal random distribution or at predefined time-points /1/.

The application environment of SIMADYN D, the digital control, requires a real time operating system with a very fast reaction time. This results from a basic sampling time that is defined via the cyclic interrupts from a timer.

The basic sampling time can be set on the timer and amounts to a minimum of 1 ms for P16 and 0.1 ms for P32.

2. Tasks

The components of an operating system are generally divided into two categories:

Control programs ensure the correct processing of the user program systems on the hardware.

Operating programs designed for creating and maintaining user program systems.

The tasks for both categories are listed below.

2.1 Components

Control Programs		SIMADYN D
Process Co-Ordination:	Task Management	
	Cyclic Interrupts	* Task Manager for T1..T5
	Acyclic Interrupts	* Task Manager for I1..I5
Memory Management:	Segmenting and Fixed Allocation	* Initialization / Memory Distribution
Input / Output Control:	Transfer from and to User Programs	Communication
	Driver	
Data Management:	Internal	* Task Manager / Buffer
		* System

The tasks marked with '*' are components of the SIMADYN D operating system core.

Operating Programs		SIMADYN D
Utility Programs:	Dialog Program	Monitor
	Test and Exception Handling	Diagnostics
	System Basic Functions	
Standard Functions:	Standard Function Blocks	

Other utility programs (editor, compiler, linker) are necessary for the generation of user programs, i.e. by utilizing the language STRUC or by generating user function blocks.

2.2 Hardware

The tasks described in section 2.1 are implemented on various hardware units:

1.	Control Programs Monitor and Utility Programs	Destination Hardware: Operating System:	Processor Module SIMADYN D
2.	User Program with Function Blocks	Destination Hardware: Operating System:	Processor Module SIMADYN D
3.	Utility Programs for Generation of User Programs	Destination Hardware: Operating System:	Programming Device, PC CP/M, MS DOS

2.3 Developing User Programs

Subsequent to the creation of the user program, on the programming device (with the aid of STRUC), the user links and locates that program with the system software and creates the required EPROMS for the destination hardware. The total system software for the destination hardware is therefore linked and located on the programming device.

3. Operating System SIMADYN D

The operating system is made up of the following components:

- Task manager for cyclic and interrupt controlled processing,
- Hardware and software initialization,
- Memory management (buffer management),
- Operating system data and lists,
- Interface to the central AMC lists,
- Link to the other components (system interfaces).

The operating system has multi processing and multi tasking mode capabilities.

The basic functions of the operating system are embedded into the total system, whereby the most important interfaces to the environment are simultaneously shown.

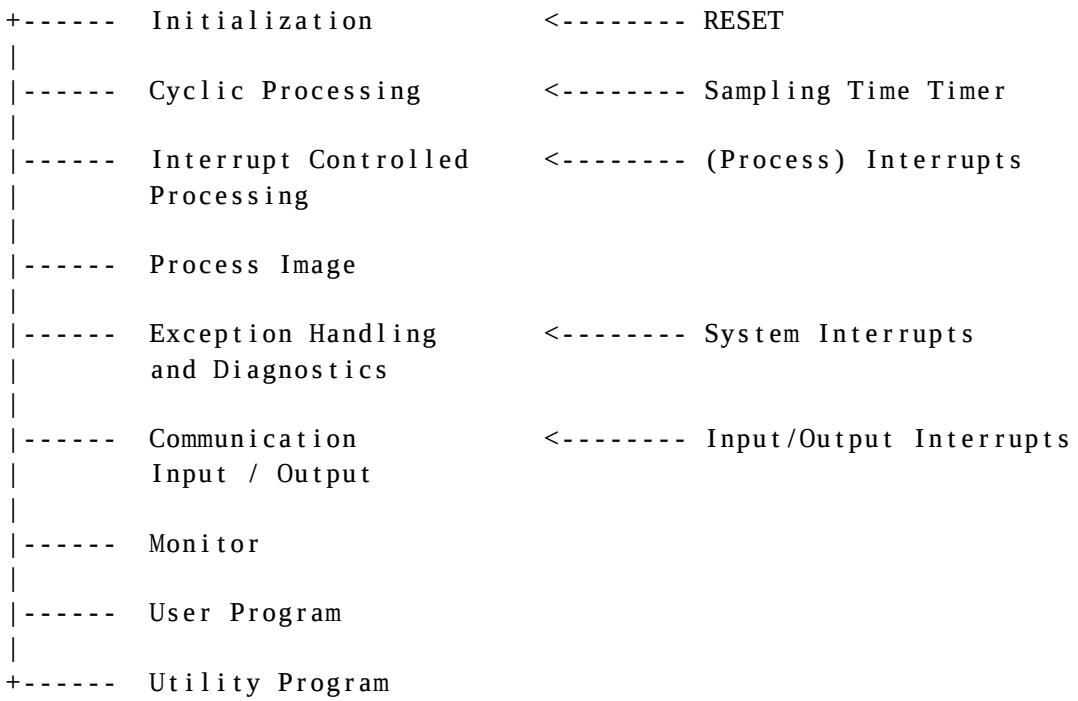

Diagram 2

3.1 Multi Processing Mode

The SIMADYN D hardware possesses the possibility of utilizing several processors for a user system (multi processing mode). Each processor module board is equipped with both system and user software. The operating system software is essentially identical on each processor module board.

The inter-processor board communication is exclusively processed, during normal mode, with the aid of the data areas of the C and L bus coupling memory. The C or L bus interrupts are also utilized for the co-ordination, during the initialization and exception handling.

The processor module boards do not respond symmetrically. In addition to the differing hardware characteristics, the first processor module board of a bus section has the responsibility of a co-ordinated sequencing during initialization of the bus master function.

3.2 Multi Tasking Mode and Task Manager

The task manager co-ordinates the processing of tasks by the processor, corresponding to their priority. Several processes (tasks) are managed, that possess differing priorities as a result of differing sampling times in the cyclic processing or differing interrupt causes in the interrupt processing.

3.3 Initialization

The initialization is activated by switching on the power supply or by activating the RESET button and causing a reset pulse. The task of the initialization is to prepare the hardware and software such that the normal mode can be implemented. It is divided into the following main functions:

- Delete memory areas (RAM, C and L bus coupling memory),
- Assign interrupt vectors,
- Initialize the hardware and peripherals with the aid of the initialization blocks (IBs),
- Set timer parameters,
- Distribute RAM memory for
  - Stack,
  - Components of the user program,
  - (Function packets),
  - Buffer system.

- C and L bus coupling memory distribution for system data and lists,
- Buffer systems,
- Copy data from EPROM into RAM,
- Transfer corrections from the EEPROM into the RAM,
- Predefine memory areas (RAM, C and L bus coupling memory), as well as counters, addresses, lists and control data,
- Evaluate configured sampling times,
- Implement plausibility checks on the configured data from the EPROM,
- Initialize the user program by sequencing the initialization mode of the function blocks for the cyclic and interrupt controlled tasks.

- Invoke initialization of the communication,
- Evaluate the results of the initialization run,
  - When errors occur:
    - Output messages,
  - When error free:
    - Set enable flags for the total system,
    - Enable interrupts,
- Invoke the background task for the internal monitoring and diagnostics.

3.4 Cyclic Processing

The task manager ensures that the cyclic processing of the tasks is assigned to differing sampling times. The sampling times have a relationship of the power of 2 to one another, according to:

T(i) = T(0) * (2 ** j) with T(0) as the basic sampling time,

j determines the value of the sampling time with
0 <= j < 16,
i numbers the sampling times with
0 <= i < 5.

Therefore the sampling times of 1 ms, 2 ms, 8 ms, 32 ms and 128 ms can be created from a basic sampling time of 1 ms. The basic sampling time is defined, with the aid of STRUC, during the configuring of the master program. The sampling times for the sequencing tasks are configured on the corresponding processors in the screen for the processor module in the master program.

The tasks are started with a phase shifted basic clock in order to prevent start accumulations. Therefore the start of a second, lower priority task with the basic clock is deferred. A result of the discrete distribution of the sampling times, based upon the power of 2, is that all low priority tasks are completely taken care of and never more than one lower priority sampling time will occur together with the basic clock.

The priorities of the tasks decrease with increasing sampling time.

The task manager is started with the basic sampling time clock of the sampling timer. The sampling time is determined and therefore the second lower priority task is allocated to the basic clock.

If the task to be started is of a lower priority than the interrupted task, then its start is buffered and the interrupted task continued. Otherwise the determined task is started. The status of the interrupted task is written into a task specific data area, which can seamlessly continue the processing as soon as no further higher priority task requires attention.

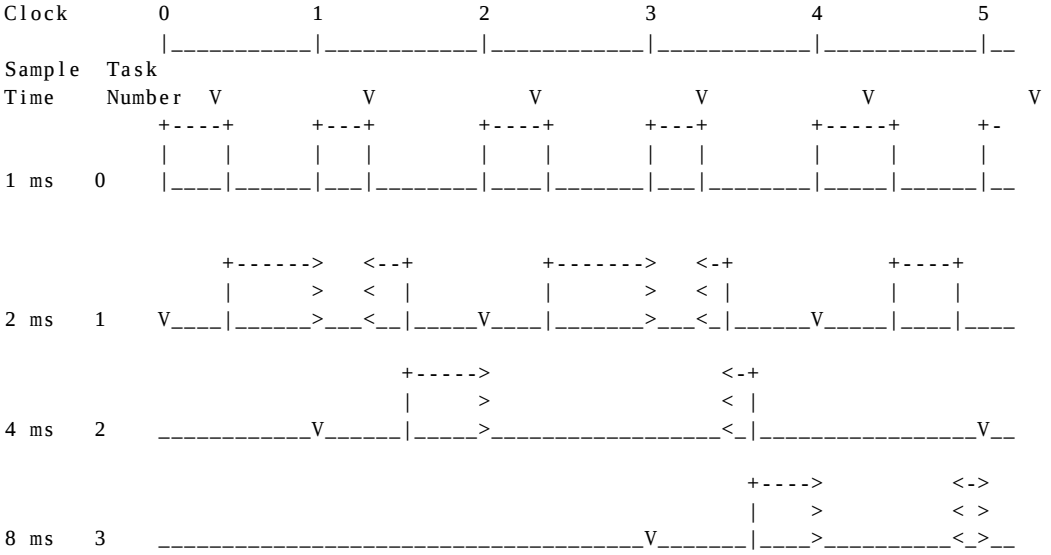

Diagram 3: Representation of the Interrupt Structure

The priority of a task increases with decreasing sampling time or rising task number. The indicated arrow "V"flags the task to be started at the predetermined time clock.

The character ">" indicates the interruption of a task, "<" its continuation.

The time component required by the operating system is not shown in this diagram. A more accurate representation would show the actual time-point of the task to be phase shifted by this time component.

3.5 Interrupt Controlled Processing

In addition to the cyclic processing, the operating system also manages tasks that are started by acyclic interrupts, especially from process interrupts. The following interrupts are possible:

- Software Interrupts,
- CPU Timer Interrupts,
- CIO Port Interrupts,
- L / C Bus Interrupts.

The priorities of the interrupts are specified by the interrupt FP configuring (I1 > I2...> I5). The user programmer configures the required interrupts, with the aid of STRUC, for his application and its processing in the interrupt controlled function packets.

3.6 Process Image (System Mode)

A check is made before starting the task processing, whether a corresponding process image must be updated. When this is the case, it is implemented before the start of the task by invoking the function blocks system mode. The update relates to:

- Binary inputs / outputs, such as the status image of the control enables and the position of the limit switches.

- Serial inputs / outputs, these are data transmitted or received via the serial interfaces with the aid of the communications software and transferred to the processing function blocks at the time-point of the process image update, i.e. a setpoint transmitted by a control.

- Analog inputs / outputs, such as values for temperature, speed, etc.

The system mode is started for both tasks to be started before processing the normal mode.

3.7 Data Exchange

The intertask communication is carried out via data areas with the aid of a buffer system in:

- Local RAM for the data exchange between tasks of a processor,
- C bus coupling memory and
- L bus coupling memory for the data exchange between tasks, that run on different processors.

The buffer system is dimensioned, for the cyclic processing, that for one generator and N users (utilizing N + 2 buffers) at least one free buffer is always available. The management of the buffer system is carried out by the operating system. Its principle is to keep a free buffer available as a write buffer and to update a read buffer for the user.

The interrupt processing has:

A local buffer area reserved on the local RAM, specifically for the data exchange between local processor interrupt controlled tasks or with cyclic tasks.

A so called "Fast" area available on the corresponding coupling memory that is utilized for the direct data exchange between interrupt controlled tasks, that are running on different processors.

The data transport is implemented by special function blocks for the data import and export.

The data consistency is ensured by a semaphore mechanism. An exception to this is only the "Fast" connections.

3.8 Monitor

The monitor is the central dialog program of the P16 processor module boards. It is an instrument for the commissioning, diagnostics and error investigation.

The monitor should be coupled to a task with average sampling time, in order to achieve satisfactory reaction times. This sampling time is configurable and must have a value of at least 32 ms.

The processing time of the monitor is uncertain, therefore tasks that are attached to it, as well as tasks with lower priority could be blocked. Therefore a time slice technology has been implemented in which the monitor is allocated a maximum processing time within its cycle (5% of the monitor sampling time).

The user interface is made up of service devices, that are controlled via communications software.

The user can access all processor module boards of the system from a dialog unit using the monitor.

The intended utilization of the monitor on a processor module board must be configured in the user program using STRUC.

3.9 Communication

The communication implements the complete input / output traffic between the hardware as well as the corresponding software components and the user interfaces. The interfaces and their parameters must be configured in the user program using STRUC.

The communication forms autonomous processes, that are controlled by input / output interrupts independently of the operating system. The implementation of the configuring for the transmission channel can be reviewed in the communication configuring description /4/.

3.10Exception Handling

SIMADYN D differentiates between errors that occur during the initialization or during the normal sequencing.

Faults occurring during the initialization usually lead to the system refusing start enables.

Faults in normal mode are separated into those that permit continuation of the operation or those that require mandatory termination of the processing.

The system informs the user concerning its status, especially the error states, using indicators on the processor module board.

Detailed information is inserted into the error data panels of the operating system when errors occur and permit an accurate error analysis.

This data can be read and altered with the aid of the monitor, as long as it is ready for operation, or by using the hex monitor.

The significance of the error signals and information can be reviewed in the manuals ‘Error Diagnostics General PM ” /2/ and ‘Error Diagnostics Communication PM ” /3/.

The handling of the hex monitor is described in /2/.

3.11 User Programs

The user program implements the technological tasks on the destination hardware. It is created on the programming device in the programming language STRUC with the aid of the available utility programs, such as editor, STRUC compiler, linker/locator and the EPROM driver.

The linker and locator processes unify the user and system software, already on the programming device, for a processor into a system. This system is subsequently programmed onto EPROMS for application on the destination hardware.

The user program can be distributed over various processor module boards, that are coupled to one another. An EPROM set must be created for each board. The distribution of the user program on the processor module boards and the linking is configured in the STRUC master program.

The STRUC source code of the user program is converted into data structures by the STRUC compiler and made available for processing on the destination hardware by the operating system.

3.12 Utility Programs

This term summarizes the system basic functions for the operating system. They include prompter functions, functions for handling the processor module displays, special test routines and interrupt routines for the handling of system errors.

3.13 Background Processing

When no tasks are currently required for processing on the processor, then it reverts to the background processing for processing the background task.

The following alternatives are available as background tasks:

- The hex monitor, utilized as a test aid.
- The on-line test mode, in which memory test routines are run.

4. P16 Processor Module Parameters

The following describes the important parameters and technical data for the total system of the P16 operating system.

4.1 Number of Processor Module Boards

The maximum number of processor module boards within a rack is 8.

A processor module board requires 2 slots. The slots not allocated to processor module boards can be assigned to peripheral boards.

4.2 Sampling Times

Number of function packets	11	
of which for the permanent processing		8
For the system diagnostics (@SIMD)	1	
For the communication	2	
Number of configurable sampling times	5	
Total number of available sampling times	16	
From basic sampling time		T(0)
To	T(0) * (2 ** 15)	
Configurable from	T(0) to 32768 * T(0)	
For example from	1 [MS] to 32.768 [S]	
Basic sampling time T(0) configurable from	1 [MS] to 16 [MS]	
	in steps of 0.1 [MS]	

4.3 Interrupts

Number of function packets		1
Number of configurable interrupts		5
Total number of available interrupts		14
Of these	Software Interrupts	8
	CPU Timer Interrupts	2
	CIO Port Interrupts	2
	Bus Interrupts	2

4.4 Operating System Processing Times

The run times of the operating system are based upon the following:

8 MHz P16 processor with sub–module MS3.

The processing time is reduced by approximately half for the 16 MHz processors.

A further acceleration of approximately 10 to 20% may be expected when utilizing the MS31, MS4 or MS45 sub–modules.

The signals, fed via the L and/or C bus, represent an approximate constant system loading since the bus clock runs at 8 MHz.

Task of the basic sampling time (calculation bases see above!):

Time for Starting	188 us
Time for Terminating	70 us
Total	258 us

Lower Priority Task:

Starting and Terminating	113 us

Lower Priority Task,
Whereby the task of the basic sampling time is not configured:

Starting and Terminating	332 us

Additional Component

for Local Buffer System	20 us
C Bus Buffer System	20 us
L Bus Buffer System	20 us

The loading of the buffer influences the buffer systems and the degree of coupling for multi processor systems also influences the operating system run time. This signifies that the search times for free buffer space is reduced with low loading and coupling.

The higher the sampling time, the smaller is the influence of the time required for the operating system.

Taking these factors into account, the relative time component for the operating system is shown in the following table for 5 sampling times of 1 ms to 16 ms:

Sampling Time	Without Buffer Loading	Average Buffer Loading	Full Buffer. Loading
1 ms	26%	43%	53%
2 ms	5%	14%	19%
4 ms	2.5%	7%	10%
8 ms	1.2%	3.5%	5%
16 ms	0.6%	1.7%	2.5%

4.5 Memory Data

Processor Module:	RAM	Max. 128 k Byte
Memory Sub-Module:	EPROM / RAM	Max. 512 k Byte
	EEPROM	Max. 8 k Byte
Coupling Memory:	L / C Bus	Max. 64 k Byte

4.6 Memory Requirements of the Operating System

The operating system has its code located in the EPROM area on the processor module board. The data is located in the RAM area.

It requires approximately:

RAM Area:	5 K Byte	
EPROM Area:	13 K Byte	for the initialization
	2 K Byte	for the cyclic sequencing
	6 K Byte	for the hex monitor
	1 K Byte	for miscellaneous, version number etc.
Total	22 K Byte	

The operating system initially utilizes the C bus and the L bus coupling memory on the coupling memory board:

approximately 1 K Byte,

as a area for managing the operating system lists.

In addition, memory is required for the buffer system and further components, i.e. the communication.

4.7 Operating System Version

The operating system can be identified by a version parameter.

A text is inserted in the following form at the absolute address segment = 0FFE0h and offset = 0 (in memory sub-module):

yymmddVxyz with yy: Year, mm: Month, dd: Day
"V": Version
xzy: Versions Number

i.e. for the version 4.0 '950401V420".

5. Literature

/1/ Schneider J.: Lexikon der Informatik und Datenverarbeitung (Data Processing Dictionary), Published by: R. Oldenbourg, 2nd. Print 1986.

/2/ User Manual,
Service, Diagnostics, Commissioning,
Error Diagnostics general PM.

/3/ User Manual,
Service, Diagnostics, Commissioning,
Error Diagnostics Communication PM.

/4/ User Manual,
Communication Configuring.